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FIG. 1

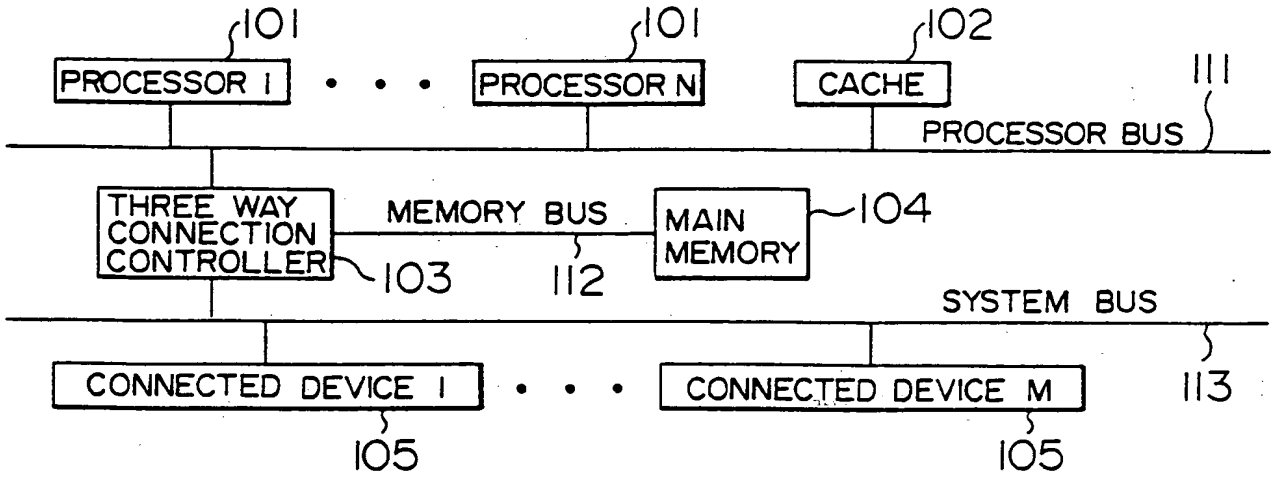


FIG. 2
PRIOR ART

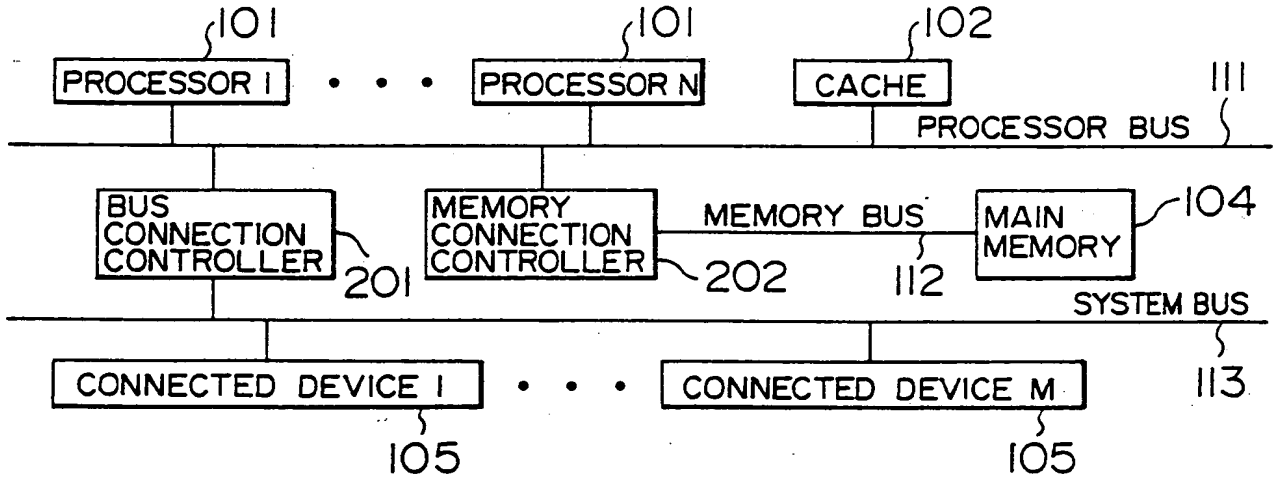


FIG. 3
PRIOR ART

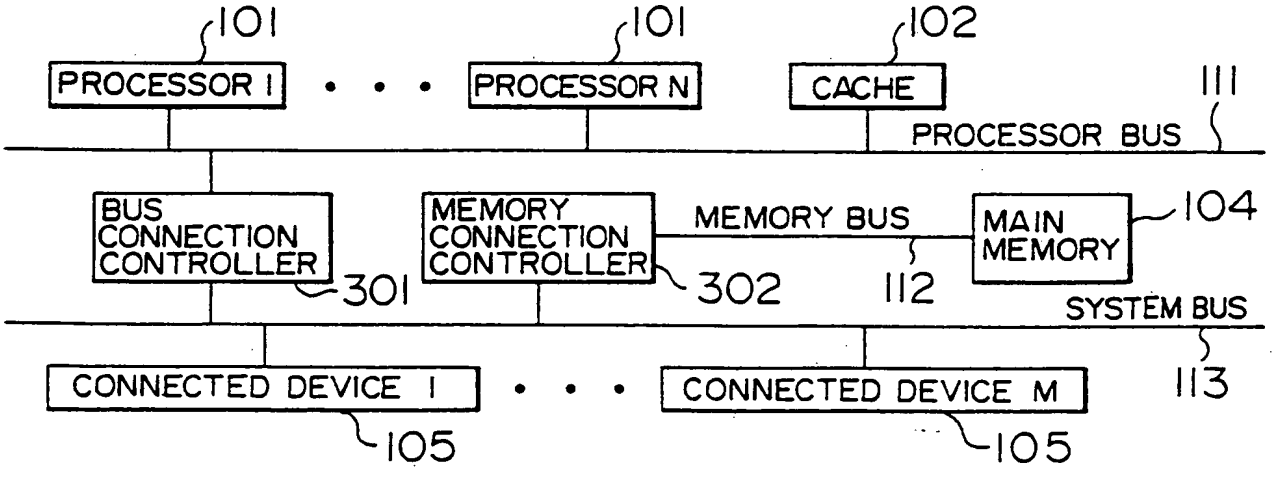


FIG. 4

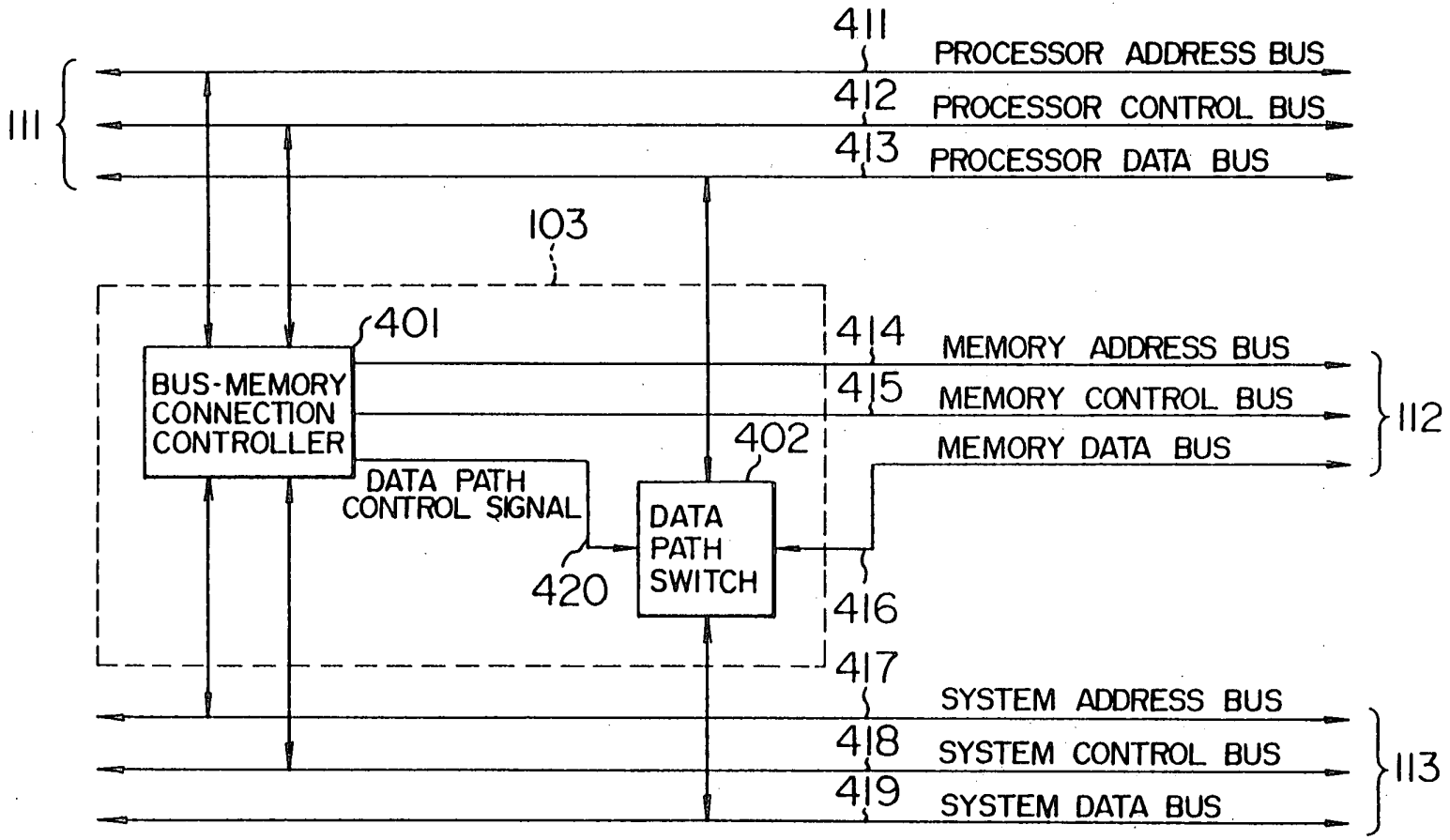

411
PROCESSOR ADDRESS BUS
412
PROCESSOR CONTROL BUS
413
PROCESSOR DATA BUS
111
103
401
BUS-MEMORY CONNECTION CONTROLLER
414
MEMORY ADDRESS BUS
415
MEMORY CONTROL BUS
MEMORY DATA BUS
112
402
DATA PATH CONTROL SIGNAL
420
DATA PATH SWITCH
416
417
SYSTEM ADDRESS BUS
418
SYSTEM CONTROL BUS
419
SYSTEM DATA BUS
113

FIG. 5

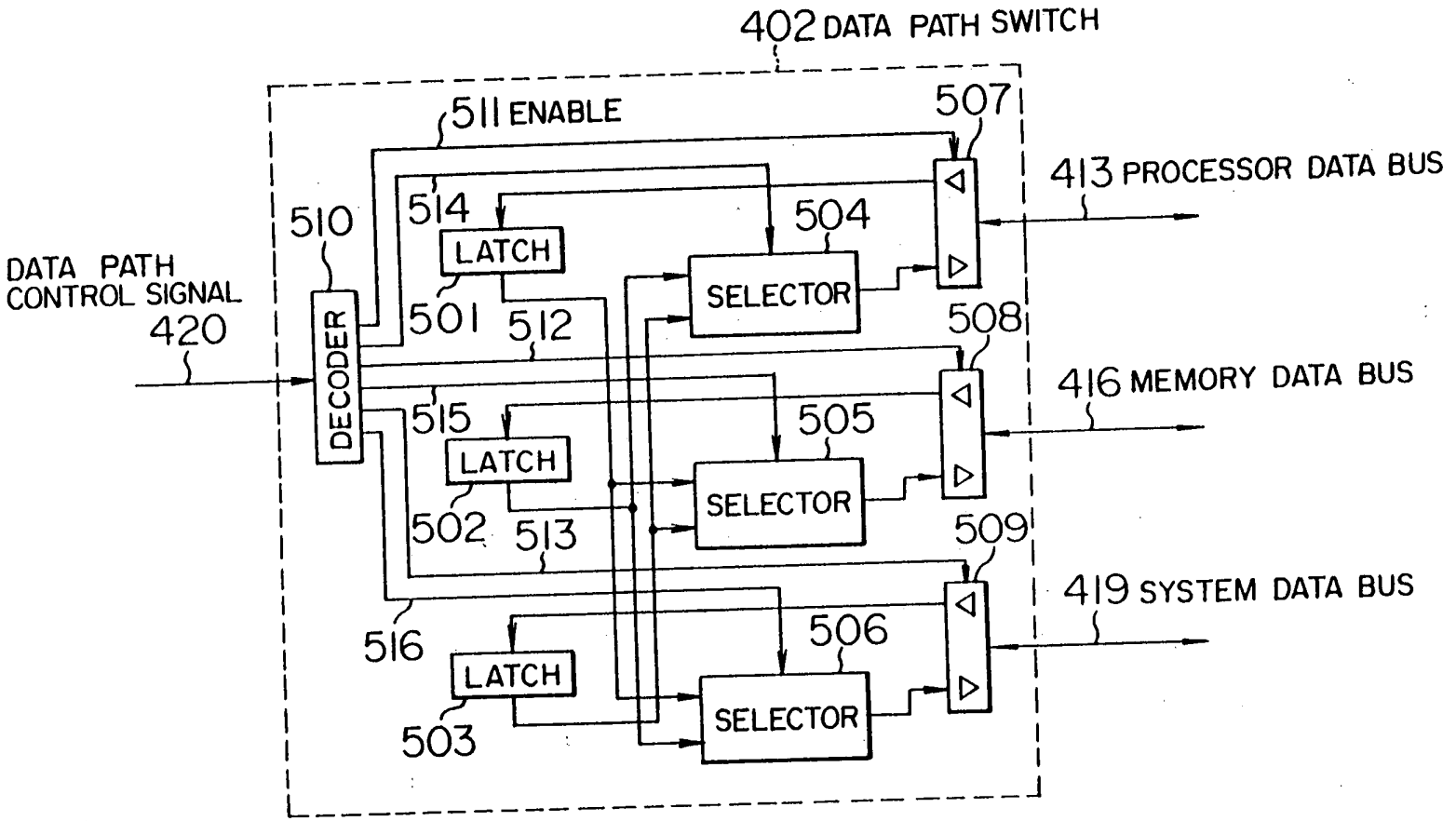

402 DATA PATH SWITCH
511 ENABLE
507
413 PROCESSOR DATA BUS
510
514
504
LATCH
SELECTOR
DATA PATH
CONTROL SIGNAL
420
DECODER
501
512
508
416 MEMORY DATA BUS
515
505
LATCH
SELECTOR
502
513
509
419 SYSTEM DATA BUS
516
506
LATCH
SELECTOR
503

FIG. 6

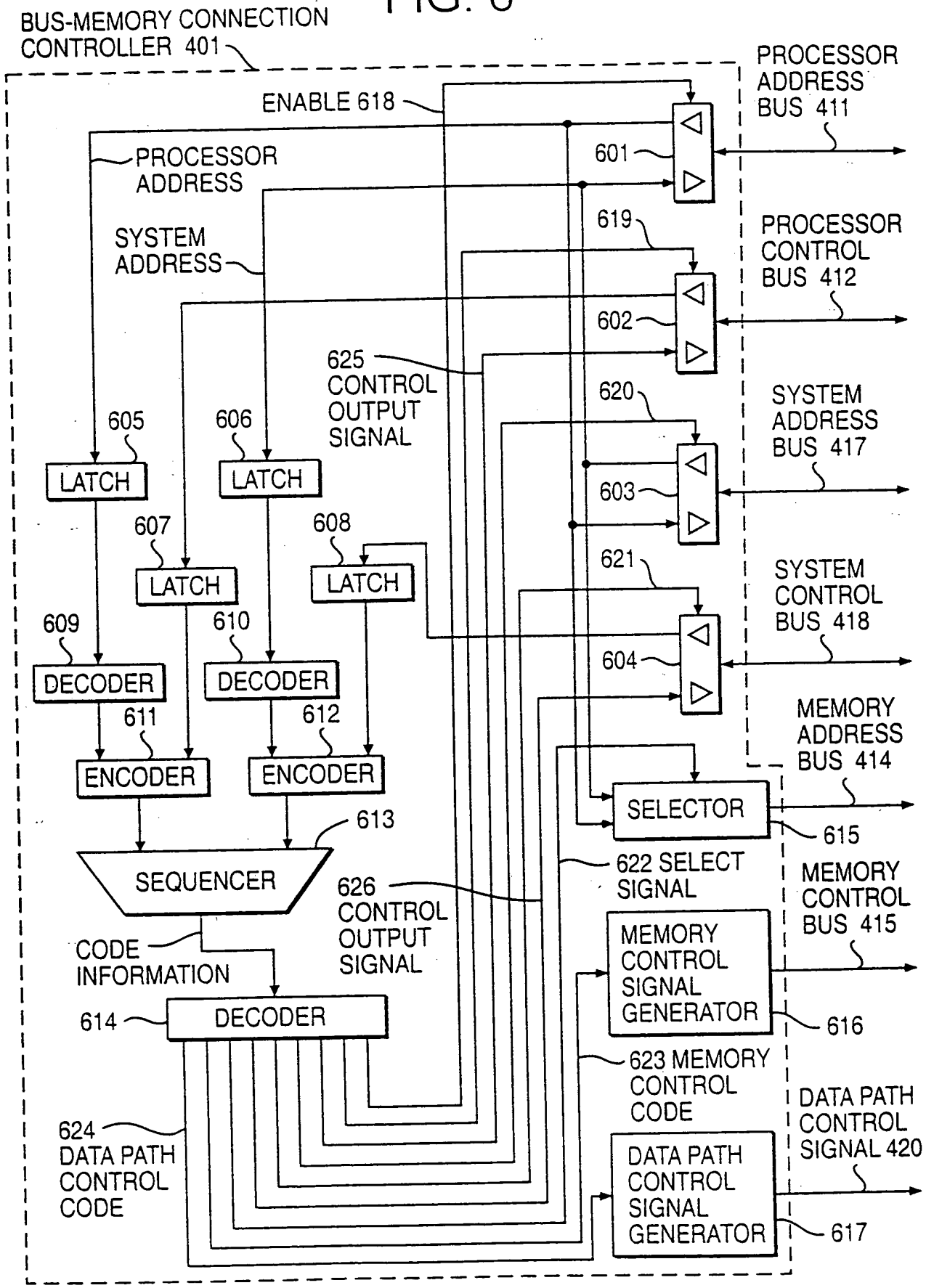

BUS-MEMORY CONNECTION CONTROLLER 401
ENABLE 618
PROCESSOR ADDRESS
SYSTEM ADDRESS
625 CONTROL OUTPUT SIGNAL
605
606
607
608
609
610
611
612
613
LATCH
LATCH
LATCH
LATCH
DECODER
DECODER
ENCODER
ENCODER
SEQUENCER
CODE INFORMATION
614
DECODER
624 DATA PATH CONTROL CODE
626 CONTROL OUTPUT SIGNAL
601
602
603
604
619
620
621
PROCESSOR ADDRESS BUS 411
PROCESSOR CONTROL BUS 412
SYSTEM ADDRESS BUS 417
SYSTEM CONTROL BUS 418
MEMORY ADDRESS BUS 414
SELECTOR
615
622 SELECT SIGNAL
MEMORY CONTROL BUS 415
MEMORY CONTROL SIGNAL GENERATOR
616
623 MEMORY CONTROL CODE
DATA PATH CONTROL SIGNAL 420
DATA PATH CONTROL SIGNAL GENERATOR
617

FIG. 7

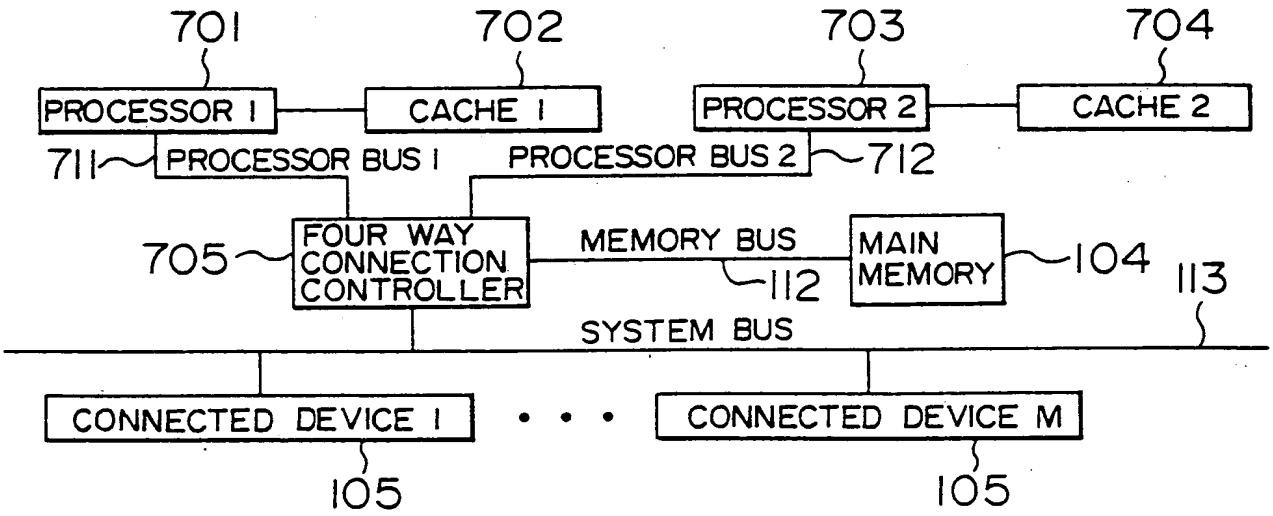

701
702
703
704
PROCESSOR 1
CACHE 1
PROCESSOR 2
CACHE 2
711
PROCESSOR BUS 1
PROCESSOR BUS 2
712
705
FOUR WAY CONNECTION CONTROLLER
MEMORY BUS
112
MAIN MEMORY
104
113
SYSTEM BUS
CONNECTED DEVICE 1
CONNECTED DEVICE M
105
105

FIG. 8

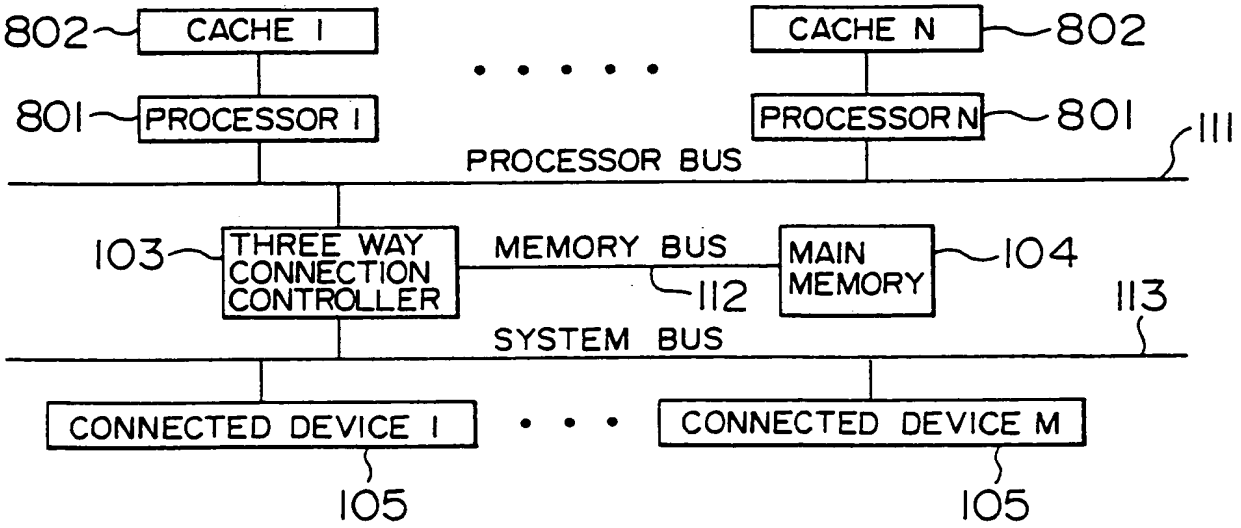

802
CACHE 1
CACHE N
802
801
PROCESSOR 1
PROCESSOR N
801
111
PROCESSOR BUS
103
THREE WAY CONNECTION CONTROLLER
MEMORY BUS
112
MAIN MEMORY
104
113
SYSTEM BUS
CONNECTED DEVICE 1
CONNECTED DEVICE M
105
105

FIG. 9

MASTER	SLAVE	READ /WRITE	DIR_P	DIR_M	DIR_S	SEL_P	SEL_M	SEL_S	DT_CNT
NUMBER IN FIG.5			511	512	513	514	515	516	420
IDLE			0	0	0	0	0	0	000
PROCESSOR 101	MAIN MEMORY 104	R	1	0	0	0	0	0	001
PROCESSOR 101	MAIN MEMORY 104	W	0	1	0	0	0	0	010
PROCESSOR 101	SYSTEM BUS DEVICE 105	R	1	0	0	1	0	0	011
PROCESSOR 101	SYSTEM BUS DEVICE 105	W	0	0	1	0	0	0	100
SYSTEM BUS DEVICE 105	MAIN MEMORY 104	R	0	0	1	0	0	1	101
SYSTEM BUS DEVICE 105	MAIN MEMORY 104	W	0	1	0	0	1	0	110

FIG. 10

PROCESSOR MAIN MEMORY READ

	DT_CNT	$\overline{ACK}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	AD_MPX	$\overline{S\_GNT}$	$\overline{S\_STB}$	$\overline{S\_ACK}$	S_ADD	S_READ
S1	O										
S2	O										
S3	O		O								
S4	O		O			O					
S5	O		O	O		O					
S6	O		O	O		O					
S7	O	O				O					
S8											

FIG. 11

PROCESSOR MAIN MEMORY WRITE

	DT_CNT	$\overline{ACK}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	AD_MPX	$\overline{S\_GNT}$	$\overline{S\_STB}$	$\overline{S\_ACK}$	S_ADD	S_READ
S1	O										
S2	O										
S3	O		O								
S4	O		O		O	O					
S5	O	O	O	O	O	O					
S6			O	O	O						

FIG. 12

PROCESSOR SYSTEM BUS DEVICE READ

	DT_CNT	$\overline{ACK}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	AD_MPX	$\overline{S\_GNT}$	$\overline{S\_STB}$	$\overline{S\_ACK}$	S_ADD	S_READ
S1	O									O	H
S2	O							O		O	H
S3	O	O									H
S4											

FIG. 13

PROCESSOR SYSTEM BUS DEVICE WRITE

	DT_CNT	$\overline{ACK}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	AD_MPX	$\overline{S\_GNT}$	$\overline{S\_STB}$	$\overline{S\_ACK}$	S_ADD	S_READ
S1	O									O	L
S2	O									O	L
S3	O							O		O	L
S4		O									

FIG. 14

DMA READ

	DT_CNT	$\overline{ACK}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	AD_MPX	$\overline{S\_GNT}$	$\overline{S\_STB}$	$\overline{S\_ACK}$	S_ADD	S_READ
S1	O						O				
S2	O						O				
S3	O		O				O				
S4	O		O			O	O				
S5	O		O	O		O	O				
S6	O		O	O		O	O				
S7	O		O	O		O	O				
S8	O		O	O		O	O		O		
S9											

FIG. 15

DMA WRITE

	DT_CNT	$\overline{ACK}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	AD_MPX	$\overline{S\_GNT}$	$\overline{S\_STB}$	$\overline{S\_ACK}$	S_ADD	S_READ
S1	O						O				
S2	O						O				
S3	O		O				O				
S4	O		O		O	O	O				
S5	O		O	O	O	O	O		O		
S6			O	O	O						

FIG. 16

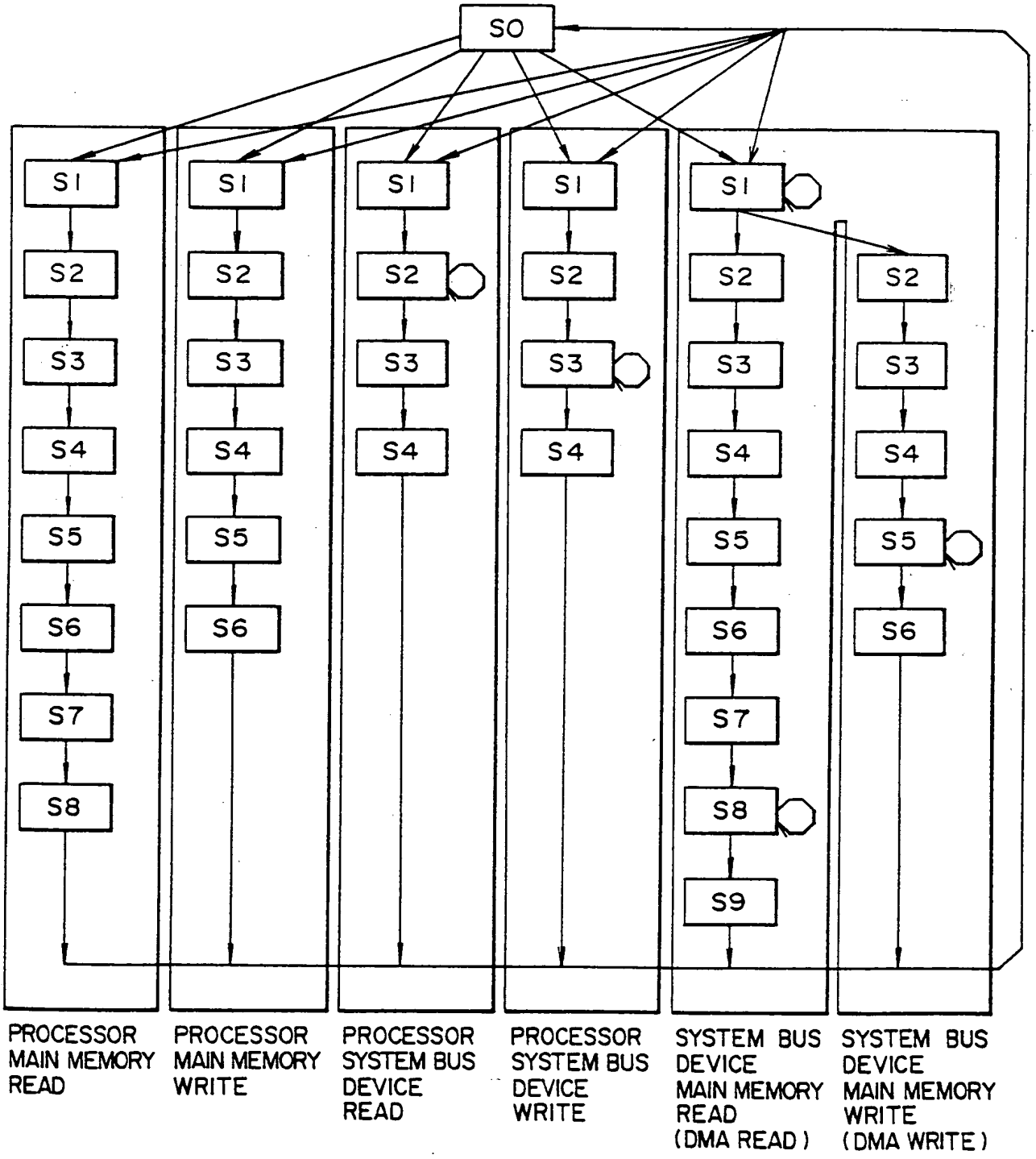

S0
S1
S2
S3
S4
S5
S6
S7
S8
S9
PROCESSOR MAIN MEMORY READ
PROCESSOR MAIN MEMORY WRITE
PROCESSOR SYSTEM BUS DEVICE READ
PROCESSOR SYSTEM BUS DEVICE WRITE
SYSTEM BUS DEVICE MAIN MEMORY READ (DMA READ)
SYSTEM BUS DEVICE MAIN MEMORY WRITE (DMA WRITE)

FIG. 17

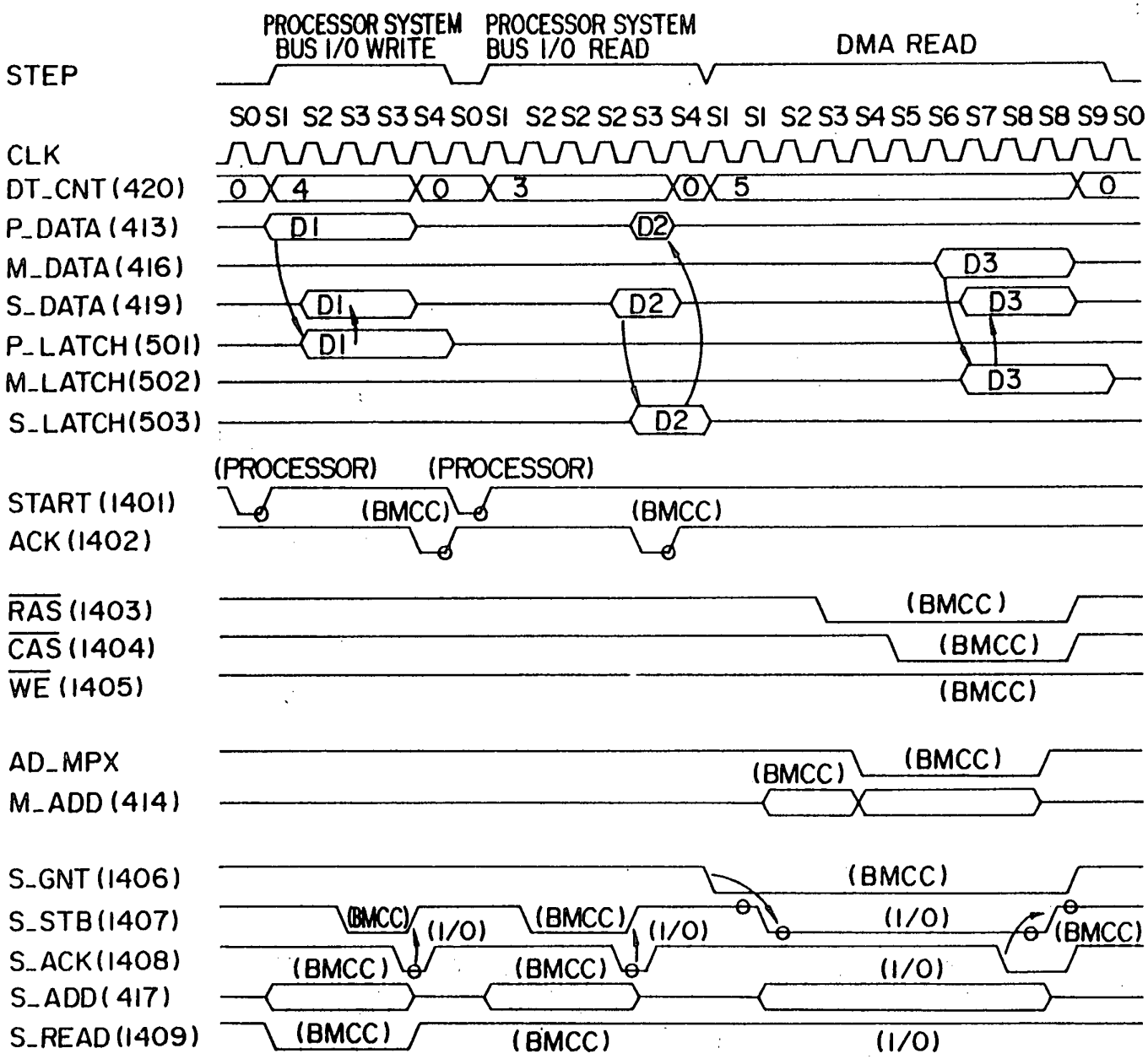

PROCESSOR SYSTEM BUS I/O WRITE
PROCESSOR SYSTEM BUS I/O READ
DMA READ
STEP
S0 S1 S2 S3 S3 S4 S0 S1 S2 S2 S2 S3 S4 S1 S1 S2 S3 S4 S5 S6 S7 S8 S8 S9 S0
CLK
DT_CNT (420)
0 4 0 3 0 5 0
P_DATA (413)
M_DATA (416)
S_DATA (419)
P_LATCH (501)
M_LATCH (502)
S_LATCH (503)
D1
D2
D3
(PROCESSOR)
(BMCC)
START (1401)
ACK (1402)
RAS (1403)
CAS (1404)
WE (1405)
AD_MPX
M_ADD (414)
S_GNT (1406)
S_STB (1407)
S_ACK (1408)
S_ADD (417)
S_READ (1409)
(I/O)

FIG. 18

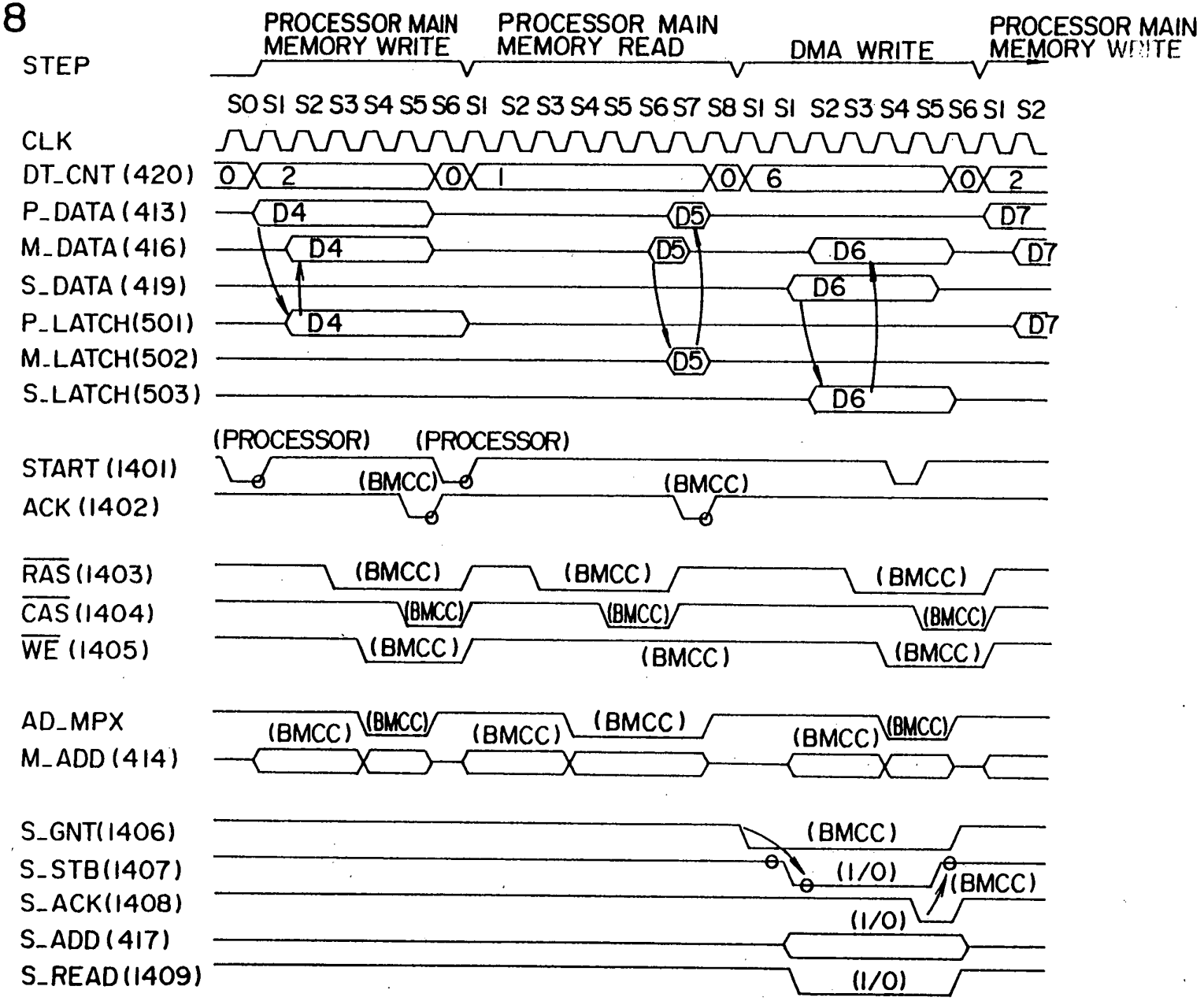
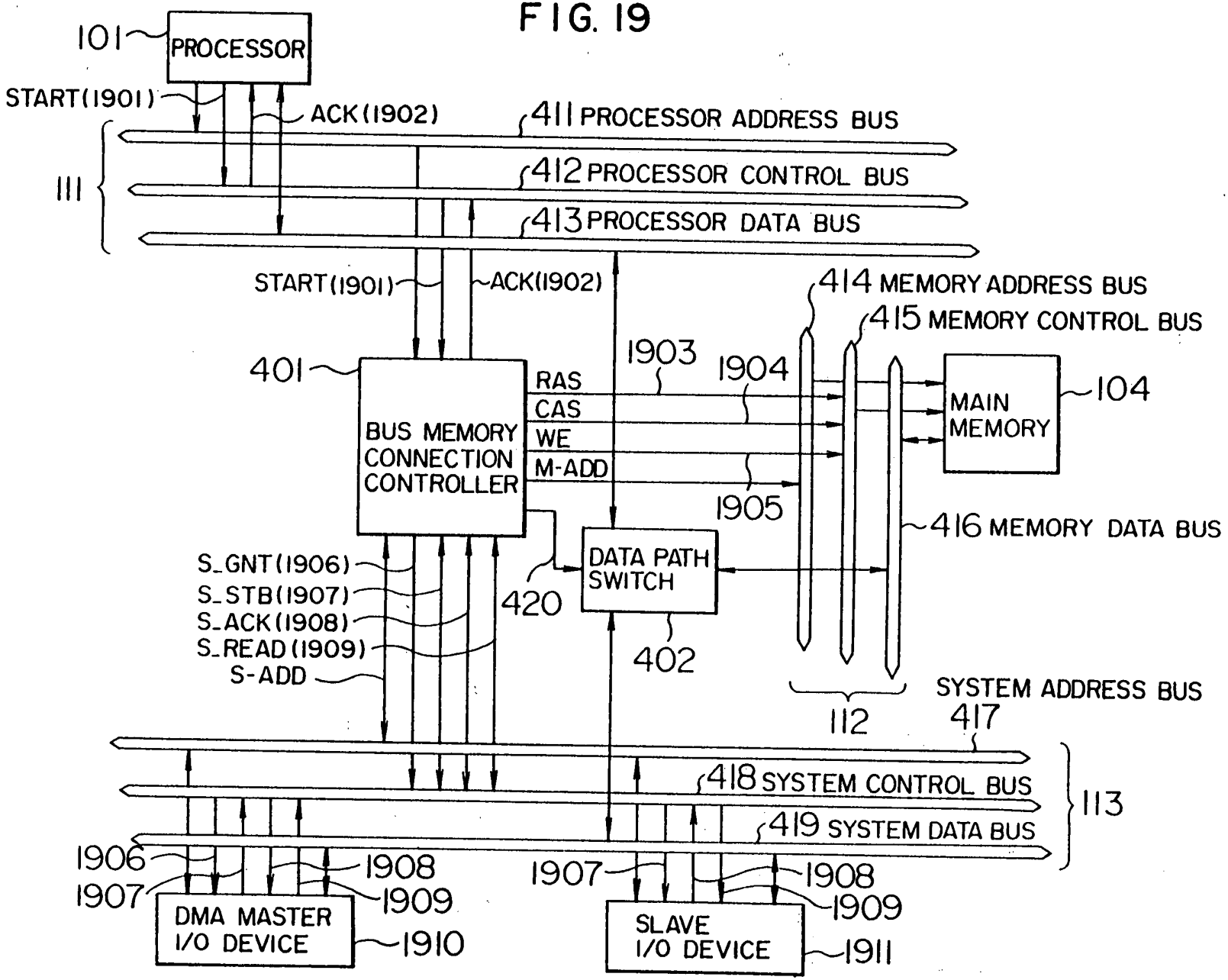

PROCESSOR MAIN MEMORY WRITE
PROCESSOR MAIN MEMORY READ
DMA WRITE
PROCESSOR MAIN MEMORY WRITE
STEP
S0 S1 S2 S3 S4 S5 S6 S1 S2 S3 S4 S5 S6 S7 S8 S1 S1 S2 S3 S4 S5 S6 S1 S2
CLK
DT_CNT (420)
P_DATA (413)
M_DATA (416)
S_DATA (419)
P_LATCH(501)
M_LATCH(502)
S_LATCH(503)
D4
D5
D6
D7
(PROCESSOR)
(BMCC)
START (1401)
ACK (1402)
RAS (1403)
CAS (1404)
WE (1405)
AD_MPX
M_ADD (414)
S_GNT(1406)
S_STB(1407)
S_ACK(1408)
S_ADD (417)
S_READ(1409)
(I/O)

FIG. 19


101
PROCESSOR
START(1901)
ACK(1902)
411 PROCESSOR ADDRESS BUS
412 PROCESSOR CONTROL BUS
413 PROCESSOR DATA BUS
111
START(1901)
ACK(1902)
414 MEMORY ADDRESS BUS
415 MEMORY CONTROL BUS
401
BUS MEMORY CONNECTION CONTROLLER
RAS
CAS
WE
M-ADD
1903
1904
1905
MAIN MEMORY
104
416 MEMORY DATA BUS
S_GNT(1906)
S_STB(1907)
S_ACK(1908)
S_READ(1909)
S-ADD
420
DATA PATH SWITCH
402
112
SYSTEM ADDRESS BUS
417
418 SYSTEM CONTROL BUS
419 SYSTEM DATA BUS
113
1906
1907
1908
1909
DMA MASTER I/O DEVICE
1910
1907
1908
1909
SLAVE I/O DEVICE
1911